

Daniel Holcomb

CONTACT INFORMATION

309H Knowles Engineering Building
151 Holdsworth Way
Amherst, MA 01003-9284

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<http://people.umass.edu/dholcomb/>

RESEARCH INTERESTS

Embedded Systems Security, Applied Formal Methods, Physical Unclonable Functions, Cyber-Physical Systems, On-chip Networks, Approximate Computing

EDUCATION

UC Berkeley, Berkeley, CA USA

Ph.D., EECS, December 2013

- Dissertation: *Formal Verification and Synthesis for Quality-of-Service in On-Chip Networks*
- Adviser: Sanjit A. Seshia, EECS
- Major: Design of Electronic Systems
- Minors: VLSI; Industrial Engineering and Operations Research

UMass Amherst, Amherst, MA USA

M.S., ECE, September 2007

- Thesis: *Chip ID and True Random Number Generation*
- Adviser: Wayne P. Bursleson, ECE

B.S., ECE, *Summa Cum Laude*, September 2005

- Thesis: *Payload Design for Atmospheric Research Balloon*
 - Adviser: Paul B. Voss, Geosciences
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ACADEMIC APPOINTMENTS

UMass Amherst, Amherst, MA USA

Assistant Professor

Jan 2015 - Present

University of Michigan, Ann Arbor, MI USA

Research Fellow

Oct 2013 - Dec 2014

UC Berkeley, Berkeley, CA USA

Graduate Student Researcher

Spring 2007 - Summer 2013

UMass Amherst, Amherst, MA USA

Graduate Research Assistant, ECE

Fall 2005 - Summer 2007

Undergraduate Research Assistant, Atmospheric Research Lab

Summer 2004 - Summer 2005

Smith College, Northampton, MA USA

Consultant, Atmospheric Research Lab

Fall 2005

INDUSTRY APPOINTMENTS

Virta Labs, Ann Arbor, MI USA

Hardware Engineering Lead

Jan 2014 - Jan 2017

Embedded systems research and development at security startup

Intel, Hillsboro, OR USA

Technology Transfer Intern - Strategic CAD Lab

Summer 2011; Summer 2012 - Spring 2013

Microarchitectural synthesis and formal verification for on-chip networks

Intel, Hudson, MA USA

Graduate Technical Intern

Spring-Summer 2006; Summer 2007

Analysis and mitigation of particle-strike induced errors in combinational circuits and memories

TEACHING

UMass Amherst, Amherst, MA USA

ECE622: Modeling and Verification of Embedded Systems

Spring 2015/6/7/8

Mezzanine level embedded systems course using Lee and Seshia textbook. Labs focus on reachability analysis.

ECE591CF: Cybersecurity Lecture Series

Fall 2015/6/8

Co-organized 1-credit seminar course featuring weekly guest speakers

ECE353: Computer Systems Lab

Fall 2015/6/7/8

Undergraduate course on applied embedded systems. Prototyping systems on breadboards using Verilog (Altera CPLD) and C programming (ATmega32)

ECE296/ECE396: Embedded Capture The Flag Competition (Independent Study)

Spring 2016/7

Organized and supervised team of undergraduate CS and ECE students in semester-long hacking competition conducted by MITRE (18 students participated for credit over the two years).

Senior Design Project

2015/6/7/8

Supervised undergraduate teams on their year-long design projects

ECE696: Independent Study

- Harshavardhan Ramanna, Fall 2017
“Hardware Design for Test Chip Evaluation of Bitline PUF”
- Mohammad Aftab Usmani, Spring 2016
“Evaluation of the feasibility of implementing Anderson PUF using SLICE-L cells on Virtex 7 FPGA”
- Abhinav Khandelwal, Fall 2015
“Design Space Exploration of Error Correction Techniques for Physical Unclonable Functions”

ECE499: Capstone Honors Project

Supervised year-long capstone project of Commonwealth College students

- Richard Hartnett (2018)
“Evaluation of Security of AES-128 WDDL Implementation on FPGA”
- Thomas Baim (2018)
“Image Processing and Phone Application Development for Mobile Phone Microscopy and Microfluidics”
- Omid Meh (2016):
“Automated Mussel Detection Using Mobile Phone Microscopy and Microfluidic Techniques”

PUBLICATIONS

Bold font in author listing denotes students for which I am the primary or co-primary research adviser.

BOOK CHAPTERS

D Holcomb “Nanoscale CMOS Memory-based Security Primitive Design”, Book chapter in: *Security Opportunities in Nano Devices and Emerging Technologies*, M. Tehranipoor, D. Forte, G. Rose, S. Bhunia (Eds.), Publisher: CRC Press/Taylor & Francis, 2017.

PEER-REVIEWED JOURNAL ARTICLES

X Xu, **S Keshavarz**, D Forte, M Tehranipoor, D Holcomb “Bimodal Oscillation as a Mechanism for Autonomous Majority Voting in PUFs”, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 2018 (to appear).

A Shanmugam, **M Usmani**, A Mayberry, DL Perkins, DE Holcomb “Imaging systems and algorithms to analyze biological samples in real-time using mobile phone microscopy”, *PLoS one*, Mar. 2018.

S Keshavarz, C Yu, S Ghandali, X Xu, D Holcomb “Survey on Applications of Formal Methods in Reverse Engineering and Intellectual Property Protection”, *Journal of Hardware and Systems Security*, pp 1-11, Aug. 2018.

R Zhang, H Jiang, ZR Wang, P Lin, Y Zhuo, D Holcomb, DH Zhang, JJ Yang, Q Xia “Nanoscale diffusive memristor crossbars as physical unclonable functions”, *Nanoscale*, pp 2721-2726, Jan. 2018.

SN Dhanuskodi, D Holcomb, “Techniques to Reduce Switching and Leakage Energy in Unrolled Block

Ciphers”, *IEEE Transactions on Computers*, Aug. 2017.

C. Yu, **X. Zhang**, **D. Liu**, M. Ciesielski, D. Holcomb, “Incremental SAT-based Reverse Engineering of Camouflaged Logic Circuits”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, pp 1647-1659, Jan. 2017

A. Vijayakumar, V.C. Patil, D.E. Holcomb, C. Paar, S. Kundu, “Physical Design Obfuscation of Hardware: A Comprehensive Investigation of Device and Logic-Level Techniques”, *IEEE Transactions on Information Forensics and Security (TIFS)*, pp 64-77, Aug. 2016

J. Hester, N. Tobias, A. Rahmati, L. Sitanayah, D. Holcomb, K. Fu, W.P. Bursleson, J. Sorber. “Persistent Clocks for Batteryless Sensing Devices”, *ACM Trans. Embed. Comput. Syst.* 15, 4, Article 77, pp 1-28, Aug. 2016

X. Xu, A. Rahmati, D. Holcomb, K. Fu, W. Bursleson “Reliable Physical Unclonable Functions using Data Retention Voltage of SRAM Cells”, *Transactions on Computer-Aided Design of Integrated Circuits and Systems*, pp 903-914, Jun. 2015

D. Holcomb, S. Seshia, “Compositional Performance Verification of NoC Designs”, *Transactions on Computer-Aided Design of Integrated Circuits and Systems*, pp 1370-1383, Sep. 2014

R. A. Zaveri, P. B. Voss, C. M. Berkowitz, E. Fortner, J. Zheng, R. Zhang, R. J. Valente, R. L. Tanner, D. Holcomb, T. P. Hartley, L. Baran, “Overnight atmospheric transport and chemical processing of photochemically aged Houston urban and petrochemical industrial plume”, *Journal of Geophysical Research: Atmospheres*, Dec. 2010.

D. E. Holcomb, W. P. Bursleson, and K. Fu, “Power-Up SRAM State as an Identifying Fingerprint and Source of True Random Numbers” *IEEE Transactions on Computers*, Sept. 2009.

E.E. Riddle, P.B. Voss, A. Stohl, D. Holcomb, D. Maczka, K. Washburn, R.W. Talbot, “Trajectory model validation during ICARTT-2004 using newly developed altitude-controlled meteorological balloons”, *Journal of Geophysical Research: Atmospheres*, Dec. 2006.

PEER-REVIEWED PAPER IN CONFERENCE OR WORKSHOP PROCEEDINGS

S Keshavarz, F Schellenberg, B Richter, C Paar, D Holcomb, “SAT-based Reverse Engineering of Gate-Level Schematics using Fault Injection and Probing”, *IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, pp 215-220, 2018. **First Place Best Poster Award**

C Ramesh, S Patil, **SN Dhanuskodi**, G Provelengios, S Pillement, D Holcomb, R Tessier, “FPGA Side Channel Attacks without Physical Access”, *IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, 2018.
acceptance rate = 21% (22/106)

S Keshavarz, D Holcomb “Threshold-based Obfuscated Keys with Quantifiable Security against Invasive Readout”, *IEEE/ACM International Conference On Computer Aided Design (ICCAD’17)*, pp 57-64, 2017.
acceptance rate = 26% (105/399)

SN Dhanuskodi, D Holcomb “An improved clocking methodology for energy efficient low area AES architectures using register renaming”, *IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED’17)*, pp 1-6, 2017.
acceptance rate = 25% (38/152)

C. Yu, D.E. Holcomb, M. Ciesielski, “Reverse Engineering of Irreducible Polynomials in GF (2^m) Arithmetic”, *Design Automation and Test in Europe (DATE)*, pp 1562-1567, Mar. 2017.
acceptance rate = 24% (193/794)

S. Keshavarz, C. Paar, D.E. Holcomb “Design Automation for Obfuscated Circuits with Multiple Viable Functions”, *Design Automation and Test in Europe (DATE)*, pp 886-889, Mar. 2017.

S Keshavarz, D Holcomb “Privacy Leakages in Approximate Adders”, *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp 1-4, May 2017.

VC Patil, A. Vijayakumar, D Holcomb, S Kundu “Improving reliability of weak PUFs via circuit techniques to enhance mismatch”, *IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, pp 146-150, 2017.

NK Dumpala, S. Patil, D. Holcomb, R. Tessier “Energy Efficient Loop Unrolling for Low-Cost FPGAs”, *2017 IEEE 25th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, pp 117-120, 2017.

S. N. Dhanuskodi, D. Holcomb, “Energy Optimization of Unrolled Block Ciphers using Combinational Checkpointing”, *RFIDSec 2016: 12th Workshop on RFID and IoT Security*, pp 47-61, 2016

X. Xu, D.E. Holcomb, “Reliable PUF Design Using Failure Patterns from Time-Controlled Power Gating”, *Defect and Fault Tolerance in VLSI and Nanotechnology Systems Symposium (DFT)*, pp 135-140, 2016

S. Vyas, N.K. Dumpala, R. Tessier, D.E. Holcomb, “Improving the Efficiency of PUF-Based Key Generation in FPGAs using Variation-Aware Placement”, *Field Programmable Logic (FPL)*, pp 1-4, 2016

S. Ghandali, G.T. Becker, D. Holcomb, C. Paar “A Design Methodology for Stealthy Parametric Trojans and Its Application to Bug Attacks”, *Cryptographic Hardware and Embedded Systems (CHES)*, pp 625-647, 2016
acceptance rate = 20% (30/148)

S. N. Dhanuskodi, **S. Keshavarz**, D. Holcomb, “LLPA: Logic State Based Leakage Power Analysis”, *International Symposium on VLSI (ISVLSI)*, pp 218-223, 2016

X. Xu, W.P. Burleson D. Holcomb, “Using Statistical Models to Improve the Reliability of Delay-Based PUFs”, *International Symposium on VLSI (ISVLSI)*, pp 547-552, 2016

X. Xu, D. Holcomb, “A Clockless Sequential PUF with Autonomous Majority Voting”, *Great Lakes Symposium on VLSI (GLSVLSI)*, pp 27-32, 2016
acceptance rate = 25% (50/197)

D. Liu, C. Yu, **X. Zhang**, D.E. Holcomb “Oracle-Guided Incremental SAT Solving to Reverse Engineer Camouflaged Logic Circuits”, *Design Automation and Test in Europe (DATE)*, pp 433-438, Mar. 2016.
acceptance rate = 24% (199/829)

A. Rahmati, M. Hicks, D. Holcomb, K. Fu, “Probable cause: the deanonymizing effects of approximate DRAM”, *International Symposium on Computer Architecture (ISCA)*, pp 604-615, 2015
acceptance rate = 19% (58/309)

X. Xu, U. Rührmair, D. Holcomb, W. Burleson “Security Evaluation and Enhancement of Bistable Ring PUFs”, *Radio Frequency Identification: security and privacy issues (RFIDSec)*, pp 3-16, Jun. 2015

D. Holcomb, K. Fu, “Building Native Challenge-Response PUF Capability into any SRAM”, *Workshop on Cryptographic Hardware and Embedded Systems (CHES)*, pp 510-526, Sep. 2014.
acceptance rate = 26% (33/127)

A. Rahmati, M. Hicks, D. Holcomb, and K. Fu, “Refreshing Thoughts on DRAM: Power Saving vs. Data Integrity”, *Workshop on Approximate Computing Across the System Stack (WACAS)*, 2014

D. Holcomb, K. Fu, “QBF-Based Synthesis of Optimal Word-Splitting in Approximate Multi-Level Storage Cells”, *Workshop on Approximate Computing Across the System Stack (WACAS)*, 2014

U. Rührmair, D. Holcomb, “PUFs at a glance”, *Design Automation and Test in Europe (DATE)*, 2014
acceptance rate = 23% (206/890)

S. Jha, M. Talalay, D. Holcomb, U. Ogras, M. Kishinevsky, M. Klingsmith, R. De Gruijl and S. Choi,

“Automated Design Space Exploration for SoC Interconnects”, *Intel Design and Test Technology Conference (DTTC)*, 2013

D. Holcomb, A. Rahmati, M. Salajegheh, W.P. Burleson, K. Fu, “DRV-Fingerprinting: Using Data Retention Voltage of SRAM Cells for Chip Identification”, *Workshop on RFID Security and Privacy (RFIDSec)* Jul. 2012

A. Rahmati, M. Salajegheh, D. Holcomb, J. Sorber, W.P. Burleson, K. Fu, “TARDIS: Time and Remanence Decay in SRAM to Implement Secure Protocols on Embedded Devices without Clocks”, *USENIX Security Symposium*, Aug. 2012

acceptance rate = 19% (43/222)

D. Holcomb, A. Gotmanov, M. Kishinevsky, S.A. Seshia, “Compositional Performance Verification of NoC Designs”, *International Conference on Formal Methods and Models for Codesign (MEMOCODE)*, Jul. 2012

D. Holcomb, B. A. Brady, S. A. Seshia, “Abstraction-Based Performance Analysis of NoCs”, *Design Automation Conference (DAC)*, Jun. 2011

acceptance rate = 23% (156/690)

B. A. Brady, D. E. Holcomb, S. A. Seshia, “Counterexample-guided SMT-driven optimal buffer sizing”, *Design Automation and Test in Europe Conference (DATE)*, Mar. 2011

L. Lin, D. Holcomb, D. K. Krishnappa, P. Shabadi, W. Burleson, “Low-Power Sub-threshold Design of Secure Physical Unclonable Functions”, *International Symposium on Low Power Electronics and Design (ISLPED)*, Aug. 2010.

acceptance rate = 24% (48/203)

D. Holcomb, W. Li, S. A. Seshia, “Design as you see FIT: System-Level Soft Error Analysis of Sequential Circuits,” *Design Automation and Test in Europe Conference (DATE)*, Apr. 2009

acceptance rate = 25% (226/895)

V. Ambrose, W. Burleson, D. Holcomb, S. Mukherjee, J. Pickholtz, “A Fast and Accurate Method for Simulating Soft Errors in Large Combinatorial Logic Circuits”, *Intel Design and Test Technology Conference (DTTC)*, 2007

D.E. Holcomb, W.P. Burleson, and K. Fu, “Initial SRAM State as a Fingerprint and Source of True Random Numbers for RFID Tags,” *Proceedings of the Conference on RFID Security (RFIDSec)*, Jul. 2007.

SELECTED NON
PEER-REVIEWED
PUBLICATIONS AND
TALKS

D. E. Holcomb, W. Li, S. A. Seshia, “Algorithms for Green Buildings: Learning-Based Techniques for Energy Prediction and Fault Diagnosis”, *UC Berkeley Technical Report EECS-2009-138*, Oct. 2009

Voss, P.B., D.E. Holcomb, R.A. Zaveri, C.M. Berkowitz, “Integrated System Optimization of Controlled Meteorological (CMET) Balloons”, *Proceedings of AIAA’s 5th Annual Aviation Technology, Integration, and Operations (ATIO) Conference and AIAA 16th Lighter-than-air systems technology conference and balloons systems conference*, Sept. 2005.

Invited Talks and External Seminars:

- “Obfuscation and Reverse Engineering of Keys and IP,” *Ruhr University Bochum*, Germany, July 6, 2017
- “Protecting keys and IP against invasive readout,” *MIT Lincoln Lab.*, Lexington MA, May 22, 2017
- “SRAM-based Physical Unclonable Functions,” *MITRE*, Bedford MA, Nov. 20, 2015
- “SRAM-based Physical Unclonable Functions,” *WPI*, Feb. 26, 2015
- “Formal Performance Verification of NoCs,” *Gigascale Systems Research Center*, Sept. 18, 2012
- “FERNS: Fingerprint Extraction and Random Numbers from SRAM,” *TSMC*, San Jose, May 25, 2010

AWARDS

- 2018 HOST Conference Best Poster award (lead author S. Keshavarz)
- 2018 NSF CAREER
- 2016 ECE Faculty Best Hair award (as voted by IEEE Student Branch)
- Intel Division Recognition Award for Soft Error Estimation Tool

PATENTS

issued patents:

D.E. Holcomb, K. Fu. “Physical unclonable function using augmented memory for challenge-response hashing” U.S. Patent 10,038,564. 31 July 2018

D.E. Holcomb, K. Fu. “Physical unclonable function using augmented memory for challenge-response hashing” U.S. Patent 9,787,481. 10 October 2017

W.P. Burleson, S.S. Mukherjee, V. Ambrose, D.E. Holcomb. “Generalized Interlocked Register Cell.” U.S. Patent 7,529,118. 5 May 2009. (Intel)

filed patents:

Denis Foo Kune, Benjamin Andrew Ransford, Daniel Edward Holcomb “Anomaly and malware detection using side channel analysis” U.S. Patent application 15/543,234. 4 Jan 2018 (Virta Labs)

K.E. Fu, D.E. Holcomb, W.P. Burleson. “Methods and Systems for Characterizing and Identifying Electronic Devices.” U.S. Patent Application 13/930,855. 28 June 2013. (UMass)

SERVICE

Sessions and events chaired or organized:

- Program co-chair at ASHES 2018
- Session chair at DAC 2018
- Finance and Publication chair, ARITH 2018
- Co-organized Hack@DAC: The DAC 2018 Hardware Security Contest (<https://hack-dac18.trust-sysec.com/>)
- Co-organized Hack@DAC: The DAC 2017 Hardware Security Contest (<https://wp.nyu.edu/hackdac17/>)
- Co-organized NSF Workshop on Foundations of Secure and Trusted Hardware (FOSTER) 2017 (<https://wp.nyu.edu/foster/>)
- Session co-chair at DAC 2016
- Co-organized VLSI security special session at DFT 2016
- Co-organizer of New England Security Day in Sept 2015 with over 100 attendees.

Member of technical program committees:

- Cryptographic Hardware and Embedded Systems (CHES) 2016, 2019
- Design Automation Conference (DAC) 2016, 2017, 2018
- Malicious Software and Hardware in Internet of Things (Mal-IoT) 2018
- Workshop on Attacks and Solutions in Hardware Security (ASHES) 2017, 2018
- IEEE Conference on Communications and Network Security (CNS) 2016
- Workshop on RFID Security and Privacy (RFIDSec) 2015, 2016
- International Workshop on Trustworthy Embedded Devices (TrustED) 2015
- Secure Component and System Identification (SECSI) 2010

Reviewer for journals including the following:

- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems
- IEEE Transactions on VLSI Systems
- IEEE Transactions on Computers
- IEEE Transactions on Circuits and Systems
- IEEE Transactions on Dependable and Secure Computing (TDSC)
- IEEE Transactions on Information Forensics & Security (TIFS)
- IEEE Computer Architecture Letters
- Nature Electronics

Grant review:

- NSF on-site panel (2016, 2017, 2018)
- NSF 2014 ad-hoc

University and College Service:

- Director of Transfer Affairs, ECE Department (2017-)
- New/transfer Student Orientation (2015,2016,2017,2018)

- ECE Department Seminar Committee (2015,2016,2018)
- ECE Department Personnel Committee (2017)
- Member of two hiring committees (2016-7)
- Tau Beta Pi faculty adviser (2017,2018)
- Academic adviser to ECE students in NSF-funded Scholarship For Service program

GRANTS
AWARDED

“CAREER: Supply Chain Security for Integrated Circuits”

National Science Foundation

D. E. Holcomb (PI)

2/1/2018 - 1/31/2023 ; \$596,160

“Security for multi-Tenant FPGAs”

Intel Corporation

R. Tessier (PI), D.E. Holcomb (Co-PI)

11/2/2017 - ; \$90,000

“Defending against against Advanced Physical Attacks”

Raytheon

W. Burlison (PI), D.E. Holcomb (Co-PI)

9/1/2017 - ; \$50,000

“Designing Strongly Obfuscated Hardware with Quantifiable Security against Reverse Engineering”

National Science Foundation

C. Paar (PI), D.E. Holcomb (Co-PI), S. Kundu (Former Co-PI)

8/1/2016 - 7/31/2020; \$1,163,227

6/1/2018 - 8/31/2018; \$7,500 REU supplement

“SecureDust – The Physical Limits of Information Security”

National Science Foundation and Semiconductor Research Corporation

D.E. Holcomb (PI), W.P. Burlison (Co-PI), R. Tessier (Co-PI)

9/1/2016 - 8/31/2019; \$462,212

“Investigating Stealthy Hardware Trojans”

National Science Foundation

C. Paar (PI), D.E. Holcomb (Co-PI), S. Kundu (Former Co-PI)

9/1/2014 - 8/31/2018; \$499,997

“CyberCorps Scholarship for Service at the University of Massachusetts Amherst”

National Science Foundation

B. Levine (PI), W.P. Burlison (Co-PI), M. Liberatore (Co-PI), M. Getmansky Sherman (Co-PI), E. Sommers (Co-PI), E. Berger (Senior Personnel), Y. Brun (SP), L. Clarke (SP), D.E. Holcomb (SP), A. Houmansadr (SP), L. Gao (SP), K. Gile (SP), A. Guha (SP), G. Miklau (SP), A. Nagurney (SP), R. Wright (SP)

9/1/2016 - 8/31/2021; \$4,159,336

RESEARCH
ADVISING

THESES IN PROGRESS, WITH ANTICIPATED ROLE OF CHAIR OR CO-CHAIR

- Shahrzad Keshavarz (PhD, 4th year)
- Siva Nishok Dhanuskodi (PhD, 3rd year)
- Xiang Li (PhD, 1st year)
- Harshavardhan Ramanna (MS, 2nd year)
- Chethan Ramesh (MS, 2nd year; co-chair with Russell Tessier)

THESES COMPLETED, WITH ROLE OF CHAIR OR CO-CHAIR

- Neev Kiran (MS, Aug. 2018; co-chair with Sunghoon Ivan Lee; continuing in UMass CS PhD program)
- Mohammad Aftab Usmani (MS, Oct. 2017; first employment Netronome)
- Xiangyu Zhang (MS, May 2017; first employment Intel)

- Shrikant Vyas (MS, Sept. 2016; co-chair with Russell Tessier; first employment Altera)
- Richard Hartnett (BS Honors, May 2018; First employment Palo Alto Networks)
- Thomas Baim (BS Honors, May 2018; First employment BAE)
- Omid Meh (BS Honors, May 2016; First employment IBM)

THESES COMPLETED, WITH ROLE OF COMMITTEE MEMBER

- Arunkumar Vijayakumar (PhD)
- Xiaolin Xu (PhD)
- Meng-Chieh (Joe) Chiu (PhD - CS)
- Mingyu Li (PhD)
- Jiajun Shi (PhD)
- Cunxi Yu (PhD)

- Shivukumar Patil (MS)
- Yunning Li (MS)
- Sourabh Kulkarni (MS)
- Sachin Bhat (MS)
- Xue Ouyang (MS)
- Vijaya Deepak Kadirvel (MS)

- Ethan Miller (BS)
- Cyril Caparanga (BS)
- Walter Brown (BS)

NSF REUS ADVISED

- Peter Stanwicks (2018)